AMCAT Computer Architecture Questions

Question 1

Which memory device is generally made of semi-conductors?

A. RAM

B. Hard-disk

C. Floppy disk

D. CD disk

Answer: Option A

Explanation: Memory devices are usually made of semi conductors for faster manipulation of the contents.

Question 2

Register renaming is done in pipelined processors

A. as an alternative to register allocation at compile time

B. for efficient access to function parameters and local variables

C. to handle certain kinds of hazards

D. as part of address translation

Answer: Option C

Explanation: Register renaming is done to avoid data hazards

Question 3

The amount of ROM needed to implement a 4 bit multiplier is

A. 64 bits

B. 128 bits

C. 1 Kbits

D. 2 Kbits

Answer Option D

Explanation: For a 4 bit multiplier, there are 24 * 24 combinations, i.e., 28 combinations. Also, Output of a 4 bit multiplier is 8 bits. Thus, the amount of ROM needed = 28 * 8 = 211 = 2048 bits = 2Kbits

Question 4

Group A -A. Hit ratio B. Pages C. Frames D. External fragmentation

Group B -1. Logical memory 2. Compaction 3. Translation look-aside buffer 4. Physical memory

A. A-2, B-4, C-1,D-3

B. A-3, B-1,C-4, D-2

C. A-2;B-1.;C-4; D-3

D. A-1; B-3; C-4; D-2

Answer: Option B

Question 5

A RAM chip has a capacity of 1024 words of 8 bits each (1K × 8). The number of 2 × 4 decoders with enable line needed to construct a 16K × 16 RAM from 1K × 8 RAM is

A. 4

B. 5

C. 6

D. 7

Answer Option B

Explanation: RAM chip size = 1k ×8[1024 words of 8 bits each]

RAM to construct =16k ×16

Number of chips required = (16k x 16)/ (1k x 8)

$$= (16 \times 2)$$

[16 chips vertically with each having 2 chips horizontally]. So to select one chip out of 16 vertical chips, we need 4 x 16 decoder.

Available decoder is 2 x 4 decoder

To be constructed is 4 x 16 decoder

Hence 4 + 1 = 5 decoders are required.

Question 6

The _____ format is usually used to store data.

A. BCD

B. Decimal

C. Hecadecimal

D. Octal

Answer: Option A

Explanation: The data usually used by computers have to be stored and represented in a particular format for ease of use.

Question 7

Calculate the number of frames the memory will have if the page size is 4 bytes and the physical memory of 16 bytes.

A. 4 frames each 4 bytes

B. 6 frames each 1 bytes

C. 2 frames each 8 bytes

D. 1 frame 16 bytes

Answer: Option A

Explanation: Total no of frames=16/4=4 and each frame contain one page size of one page is 4 byte. You have completed 2/6

Question 8

Consider the following sequence of micro-operations.

    MBR ← PC

    MAR ← X

    PC ← Y

    Memory ← MBR

Which one of the following is a possible operation performed by this sequence?

A. Instruction fetch

B. Operand fetch

C. Conditional branch

D. Initiation of interrupt service

Answer: Option D

Question 9

The control unit controls other units by generating _____

A. Control signals

B. Timing signals

C. Transfer signals

D. Command Signals

Answer: Option B

Explanation: This unit is used to control and coordinate between the various parts and components of the CPU.

Question 10

A computer has a 256 KByte, 4-way set associative, write back data cache with block size of 32 Bytes. The processor sends 32 bit addresses to the cache controller. Each cache tag directory entry contains, in addition to address tag, 2 valid bits, 1 modified bit and 1 replacement bit. The number of bits in the tag field of an address is

A. 11

B.14

C. 16

D. 27

Answer: Option C

Explanation: A set-associative scheme is a hybrid between a fully associative cache, and direct mapped cache. It's considered a reasonable compromise between the complex hardware needed for fully associative caches (which requires parallel searches of all slots), and the simplistic direct-mapped scheme, which may cause collisions of addresses to the same slot (similar to collisions in a hash table). Number of blocks = Cache-Size/Block-Size = 256 KB / 32 Bytes = 213 Number of Sets = 213 / 4 = 211 Tag + Set offset + Byte offset = 32 Tag + 11 + 5 = 32 Tag = 16